CLAIMS

What is claimed is:

1. An adjustable, segmented amplifier, comprising:
   a) a first fixed stage configured to amplify an analog signal and provide a first amplified output at a first common node; and
   b) an adjustable stage comprising a plurality of independently selectable parallel amplifier segments, each of said parallel amplifier segments having an input at said first common node and an output at a second common node, wherein said adjustable stage is configured to provide an output signal in one of a plurality of power ranges corresponding to a number of selected parallel amplifier segments, said output signal having a minimum power efficiency when two or more of said parallel amplifier segments are selected.

2. The adjustable amplifier of Claim 1, wherein each of said parallel amplifier segments comprises a transistor having a control terminal, and said adjustable stage comprises a first inductor in electrical communication with said control terminal of at least one of said transistors.

3. The adjustable amplifier of Claim 2, wherein each of said parallel amplifier segments further comprises a capacitor in electrical communication with said first common node and said control terminal of said transistor.

4. The adjustable amplifier of Claim 1, wherein each of said parallel amplifier segments comprises (i) a transistor having a control terminal, and (ii) a first inductor in electrical communication with said control terminal of said transistor.

5. The adjustable amplifier of Claim 4, wherein each of said parallel amplifier stages further comprises a bias circuit in electrical communication with said first inductor.

6. The adjustable amplifier of Claim 1, wherein at least one of said plurality of parallel amplifier segments is selected for operation.

7. The adjustable amplifier of Claim 6, wherein said at least one selected parallel amplifier segment is selected for operation by applying a non-zero bias at a control terminal thereof.

8. The adjustable amplifier of Claim 7, further comprising a bias generator configured to apply a bias to said control terminal.

9. The adjustable amplifier of Claim 8, wherein said bias generator comprises a current mirror.

10. The adjustable amplifier of Claim 9, wherein said bias generator further comprises a buffer transistor configured to receive an output from said current mirror and provide said bias.

11. The adjustable amplifier of Claim 9, further comprising a current source.

12. The adjustable amplifier of Claim 11, wherein said current source comprises a programmable digital-to-analog converter.

13. The adjustable amplifier of Claim 1, wherein an efficiency of said high-efficiency output power range is at least 50% of a maximum efficiency of said adjustable amplifier.

14. The adjustable amplifier of Claim 13, wherein said efficiency is at least 60% of said maximum efficiency.

15. The adjustable amplifier of Claim 1, wherein said fixed stage comprises a first bipolar transistor and each of said plurality of parallel amplifier segments comprises a second bipolar transistor.

16. The adjustable amplifier of Claim 15, further comprising:
    a) a first inductor in electrical communication between said first bipolar transistor and a first electric potential; and
    b) a second inductor in electrical communication between each of said second bipolar transistors and said first electric potential.

17. The adjustable amplifier of Claim 1, wherein each of said plurality of parallel amplifier segments has substantially the same (i) size, (ii) design and/or layout, and/or (iii) gain function, output power and/or power efficiency characteristics as the others of said plurality of parallel amplifier segments.

18. A circuit, comprising:
    a) means for amplifying an analog signal to provide a first amplified signal;
    b) means for providing an adjustably amplified output from said first amplified signal; and
    c) means for selecting an output power range for said adjustably amplified output.

19. The circuit of Claim 18, wherein said means for providing said adjustably amplified output comprises a plurality of parallel, independently selectable means for further amplifying said first amplified signal, each of said parallel means for further amplifying having an input at a first common node and an output at a second common node.

20. The circuit of Claim 19, wherein said adjustably amplified output has one of a plurality of power ranges corresponding to a number of selected means for further amplifying, said output signal having a minimum power efficiency when two or more of said means for further amplifying are selected.

21. The circuit of Claim 20, having a power efficiency of at least 50% of a maximum efficiency of said circuit.

22. The circuit of Claim 19, wherein each of said means for further amplifying comprises a transistor having a control terminal, and said circuit further comprises a first means for coupling said control terminal of at least one of said transistors to a first bias.

23. The circuit of Claim 22, wherein each of said means for further amplifying further comprises a means for filtering said first amplified signal in electrical communication with said first common node and said control terminal of said transistor.

24. The circuit of Claim 19, wherein each of said means for further amplifying comprises (i) a transistor having a control terminal, and (ii) a first means for coupling said control terminal of said transistor to a bias signal.

25. The circuit of Claim 24, further comprising a means for providing said bias signal.

26. The circuit of Claim 25, wherein said means for providing said bias signal comprises a current mirror and a means for providing a current to said current mirror.

27. The circuit of Claim 26, wherein said means for providing said bias signal further comprises a means for buffering an output from said current mirror.

28. The circuit of Claim 19, wherein at least one of said plurality of means for further amplifying is selected for operation.

29. The circuit of Claim 19, wherein said means for amplifying comprises a first bipolar transistor and each of said means for further amplifying comprises a second bipolar transistor.

30. The circuit of Claim 29, further comprising:
    a) a first means for coupling an output matching network to an output of said means for amplifying; and
    b) a corresponding second means for coupling a control gate of each of said second bipolar transistors to a bias signal.

31. The circuit of Claim 19, wherein each of said means for further amplifying has substantially the same (i) size, (ii) design and/or layout, and/or (iii) gain function, output power and/or power efficiency characteristics as the other(s) of said means for further amplifying.

32. An integrated circuit, comprising:
    a) the adjustable amplifier of Claim 1; and
    b) a transmitter communicatively coupled to said adjustable amplifier, said transmitter being configured to transmit said analog signal to said adjustable amplifier.

33. The integrated circuit of Claim 32, wherein said analog signal has a frequency of at least about 800 MHz.

34. The integrated circuit of Claim 32, wherein said analog signal has a frequency of at least about 2.4 GHz.

35. A transceiver comprising of the integrated circuit of Claim 32.

36. The transceiver of Claim 35, wherein the transceiver is compliant with a standard selected from the group consisting of Institute of Electrical and Electronic Engineers (IEEE) 802.11, 802.11a, 802.11b, 802.11g, 802.11h, 802.11i, 802.11n and 802.16.

37. A system for broadcasting an analog signal, comprising:
    a) the integrated circuit of Claim 32;
    b) a signal converter configured to provide a converted analog output signal from said output signal of said adjustable amplifier; and
    c) a transmission antenna configured to broadcast said converted analog output signal.

38. The system of Claim 37, wherein said signal converter comprises a transformer.

39. The system of Claim 37, further comprising an output capacitor coupled to said second common node.

40. The system of Claim 37, further comprising an output inductor coupled to said second common node.

41. The system of Claim 40, further comprising an adjustable resistor coupled to said output inductor.

42. The system of Claim 37, wherein said output signal comprises a differential signal, and said signal converter is configured to convert said differential signal to a single-ended signal.

43. The system of Claim 42, further comprising first and second output capacitors, respectively coupled to each line of said differential output signal.

44. The system of Claim 42, further comprising first and second output inductors, respectively coupled to each line of said differential output signal.

45. The system of Claim 44, further comprising first and second adjustable resistors, respectively coupled to said first and second output inductors.

46. The system of Claim 44, further comprising a differential output capacitor, respectively coupled to each line of said differential output signal.

47. A network, comprising:
    a) the system of Claim 37; and
    b) a receiver in electromagnetic communication with said system.

48. The network of Claim 47, further comprising a receiving antenna in communication with said receiver.

49. A network, comprising:
    a) a plurality of the systems of Claim 37; and
    b) a plurality of receivers, each of said receivers being in communication with at least one of said systems.

50. The network of Claim 49, wherein at least one of said systems is in communication with at least two of said receivers.

51. The network of Claim 49, wherein at least two of said systems are in communication with at least one of said receivers.

52. An integrated circuit, comprising:
    a) the circuit of Claim 18; and
    b) a means for transmitting said analog signal to said adjustable amplifier.

53. The integrated circuit of Claim 52, wherein said analog signal has a frequency of at least about 2.4 GHz.

54. A transceiver comprising the integrated circuit of Claim 52.

55. The transceiver of Claim 54, wherein the transceiver is compliant with a standard selected from the group consisting of Institute of Electrical and Electronic Engineers (IEEE) 802.11, 802.11a, 802.11b, 802.11g, 802.11h, 802.11i, 802.11n and 802.16.

56. A system, comprising:
    a) the integrated circuit of Claim 52;
    b) a means for providing said amplified analog output signal from said output signal; and
    c) a means for broadcasting said amplified analog output signal.

57. The system of Claim 56, wherein said means for providing comprises a pair of inductors in electromagnetic communication with each other.

58. The system of Claim 56, wherein said output signal comprises a differential signal, and said means for providing is configured to convert said differential signal to a single-ended signal.

59. A network, comprising:
    a) the system of Claim 56; and
    b) a means for receiving said amplified analog output signal, in communication with said system.

60. The network of Claim 59, further comprising a means for processing said amplified analog output signal received by said means for receiving, wherein said means for processing is in communication with said means for receiving.

61. A network, comprising:
    a) a plurality of the systems of Claim 56; and
    b) a plurality of means for receiving said amplified analog output signal, each of said means for receiving being in communication with at least one of said systems.

62. The network of Claim 61, further comprising a plurality of means for processing said amplified analog output signal received by said means for receiving, wherein each of said means for processing is in communication with a unique one of said means for receiving.

63. The network of Claim 62, wherein at least one of said systems is in communication with at least two of said means for receiving.

64. The network of Claim 62, wherein at least two of said systems are in communication with at least one of said means for receiving.

65. A method of amplifying an analog signal, comprising the steps of:
    a) amplifying said analog signal in a fixed amplifier stage;
    b) selecting a number of parallel amplifier segments for subsequent signal amplification; and
    c) amplifying said amplified analog signal with said activated parallel, selectable amplifier segments to generate an output signal in a unique output power range corresponding to the number of selected parallel amplifier segments.

66. The method of Claim 65, wherein said selecting step comprises applying a bias to those amplifier segments to be selected.

67. The method of Claim 65, further comprising the step of generating said bias.

68. The method of Claim 65, further comprising the step of generating said bias independently for each selected parallel amplifier segment.

69. The method of Claim 68, wherein a value of said bias corresponds to said number of selected amplifier segments.

70. The method of Claim 69, wherein said bias is generated from a programmable current, and said method further comprises determining a value of said programmable current based on said number of selected amplifier segments.

71. The method of Claim 65, wherein said output signal has a minimum power efficiency when two or more of said parallel amplifier segments are selected.

72. The method of Claim 71, wherein said minimum power efficiency is at least 50% of a maximum efficiency of an amplifier comprising said fixed amplifier stage and said parallel amplifier segments.

73. The method of Claim 65, further comprising the step of matching a frequency of said output signal to an input of each of said parallel amplifier segments.

74. The method of Claim 65, further comprising the step of broadcasting said output signal.

75. The method of Claim 65, wherein said output signal has a minimum frequency of about 800 MHz.

76. The method of claim 65, wherein the method is compliant with a standard selected from the group consisting of Institute of Electrical and Electronic Engineers (IEEE) 802.11, 802.11a, 802.11b, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.